

LP5912 Ultra-Low-Noise, 500-mA Linear Regulator for RF and Analog Circuits – Requires No Bypass Capacitor

1 Features

- Input Voltage Range: 1.6 V to 6.5 V
- Output Voltage Range: 0.8 V to 5.5 V
- Output Current: 500 mA
- Low Output Voltage Noise: < 12 μV_{RMS}
- PSRR: 75 dB at 1 kHz
- Output Voltage Tolerance: $\pm 2\%$
- Low I_{Q} (Enabled): 12 μA
- Shutdown Supply Current < 1 μA
- Low Dropout: 100 mV at 500-mA Load
- Stable with 1- μF Ceramic Input and Output Capacitors
- Thermal-Overload and Short-Circuit Protection
- Reverse Current Protection
- No Noise Bypass Capacitor Required
- Output Discharge for Fast Turnoff
- Power Good Output
- Internal Soft-Start to Limit the Inrush Current
- -40°C to 125°C Junction Temperature Range for Operation

2 Applications

- Medium-Current, Noise-Sensitive Applications
- Battery-Powered Systems
- Radio Transceivers, PLL/Synthesizer, Clocking

3 Description

The LP5912 is a linear regulator capable of supplying 500-mA output current. Designed to meet the requirements of RF and analog circuit, the LP5912 device provides low noise, high PSRR, low quiescent current and low line and load transient response. The LP5912 offers class-leading noise performance without a noise bypass capacitor and ability for remote output capacitance placement.

The device is designed to work with a 1- μF input and a 1- μF output ceramic capacitor (no separate noise bypass capacitor is required).

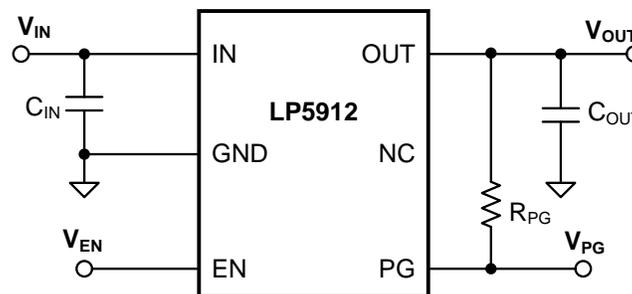
This device is available with fixed output voltages from 0.8 V to 5.5 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option needs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP5912	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the Package Option Addendum (POA) at the end of this data sheet.

Simplified Schematic



4 Device and Documentation Support

4.1 Related Documentation

For additional information, see the following:

- TI Application Note *Leadless Leadframe Package (LLP)* ([SNOA401](#))
- TI Application Report *Semiconductor and IC Package Thermal Metrics* ([SPRA953](#))
- TI Application Report *Using New Thermal Metrics* ([SBVA025](#))
- TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* ([SZZA017](#))

4.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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4.3 Trademarks

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4.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5912-0.9DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
LP5912-0.9DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	-40 to 125		
LP5912-1.5DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
LP5912-1.5DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	-40 to 125		
LP5912-1.8DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
LP5912-1.8DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	-40 to 125		
LP5912-2.8DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
LP5912-2.8DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	-40 to 125		
LP5912-3.3DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
LP5912-3.3DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

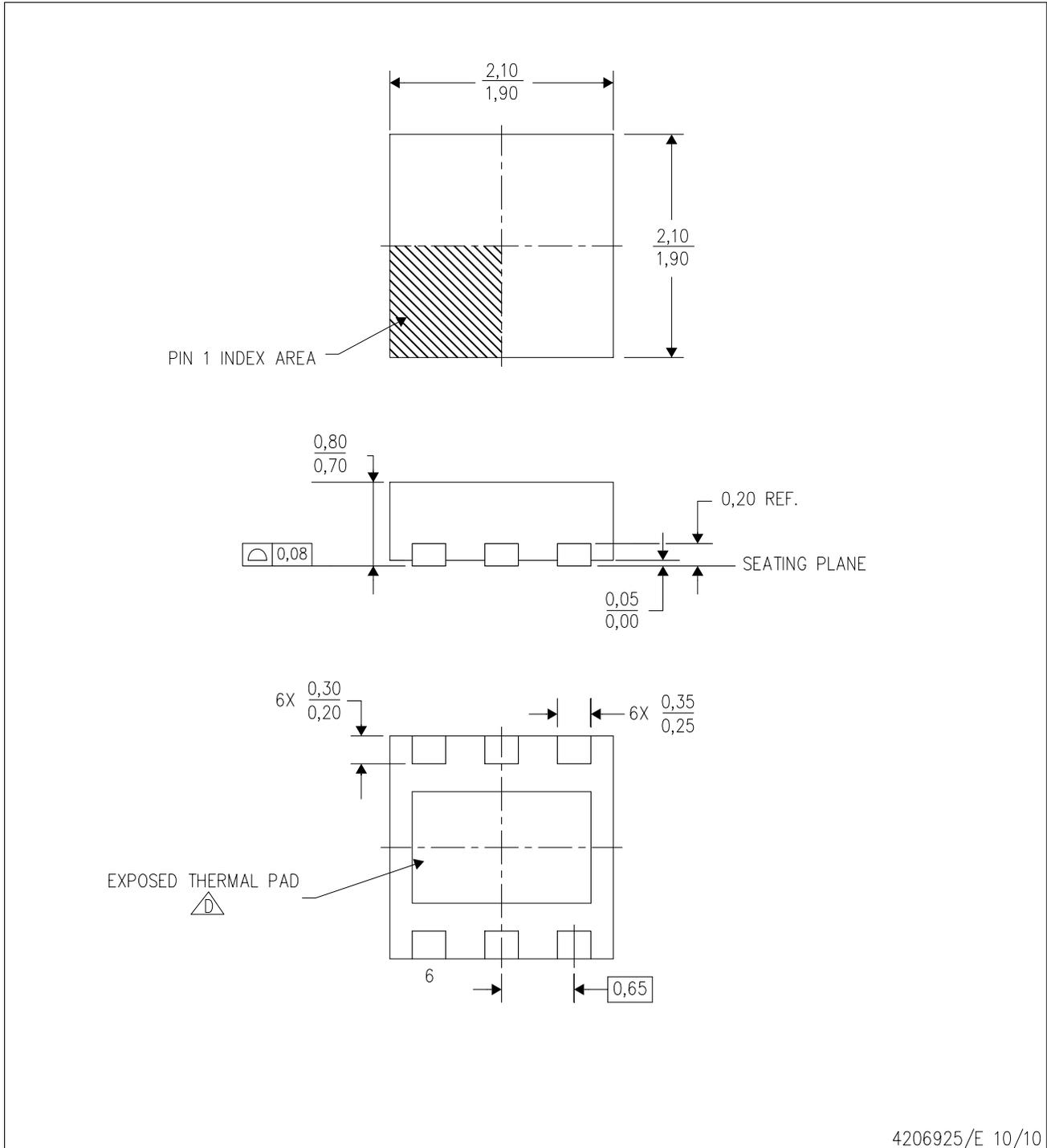
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MECHANICAL DATA

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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